# Soft Switching Symmetric Bipolar Outputs DC-Transformer (DCX) for Eliminating Power Supply Pumping of Half-Bridge Class-D Audio Amplifier

Xiang Zhou, *Member, IEEE*, Jianping Xu, *Member, IEEE*, Shu Zhong, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—A soft switching symmetric bipolar outputs dc-transformer (DCX) for eliminating power supply pumping of half-bridge class-D audio amplifiers is proposed in this paper. Compared with the traditional unidirectional front-end dc–dc converter in the half-bridge class-D audio amplifier, output capacitances of the proposed DCX and voltage stress of the half-bridge class-D audio amplifier are significantly reduced. Soft switching of the proposed DCX can be achieved when the load current of half-bridge class-D audio amplifier is positive or negative. Thus, the efficiency and power density of the proposed audio amplifier system can be improved. In addition, the proposed DCX has smoothing transition between the positive load current and the negative load current with a simple open-loop controller. The operating principle of the proposed DCX is analyzed and a 200-W prototype is built up. Experimental results show that power supply pumping is reduced with small DCX output capacitors, symmetric bipolar outputs are obtained and peak efficiency of 96.3% is achieved.**

***Index Terms*—DC-transformer, half-bridge class-D audio amplifier, soft switching, symmetric bipolar outputs.**

## I. Introduction

ALONG with the development of portable audio electronics equipment, an audio amplifier with low output voltage distortion, high efficiency, and high power-density has attracted much attention recently. Class-D audio amplifiers are thus more and more popular and start to flourish in applications where linear amplifiers once dominated [1]. Compared with linear amplifiers, modern class-D audio amplifiers benefit from small volume and high system efficiency [2].

Class-D audio amplifier can be classified into the half-bridge and full-bridge class-D audio amplifier. Compared with the full-bridge class-D audio amplifier, the half-bridge class-D audio amplifier has reduced devices number and stray inductance [3]. In order to provide a stable power supply for the half-bridge class-D audio amplifier system, high-performance front-end dc–dc converter is required [4]. Boost converter is used as a front-end dc–dc converter to provide unipolar supply for half-bridge class-D audio amplifier in [5]. However, a large dc blocking capacitor is required to prevent the speaker from being damaged by a high dc voltage, which reduced the power density of the audio amplifier system [6]. In contrast, in half-bridge class-D audio amplifier with bipolar power supplies, a bulky blocking capacitor can be removed [6], [7]. Typical half-bridge class-D audio amplifier system consists of front-end single input bipolar outputs dc–dc converter and half-bridge class-D audio amplifier. Bipolar outputs flyback converter or *LLC* resonant converter is widely used as a front-end converter [8], [9]. A voltage doubler rectified boost-integrated half-bridge class-D audio amplifier is proposed in [10], which achieves ZVS of switches and has no dc magnetizing current for the transformer.

Generally, due to ac load current and traditional unidirectional front-end dc–dc converter, the voltages across power supplies of half-bridge class-D audio amplifier have large voltage ripples, especially when output voltage frequency is low, which is called power supply pumping [4]. Severe power supply pumping significantly increases the voltage stress of the devices of class-D audio amplifier and deteriorates total harmonic distortion and noise (THD+N) of the audio amplifier system [11], [12]. In order to improve THD+N and suppress power supply pumping, some control strategies are studied to obtain high power supply rejection ratio (PSRR) [13]–[15]. In general, the large bulky electrolytic capacitor is used as the filter of the front-end dc–dc converter to reduce supply voltage ripple of the half-bridge class-D audio amplifier system, which reduces the power density of the audio amplifier system.

Compared with the large bulky electrolytic capacitor in a unidirectional front-end dc–dc converter, bidirectional front-end dc–dc converter can transfer feedback energy to input power supply of the audio amplifier system, which reduces the output capacitor of the dc–dc converter and increases the power density [16]. In a bidirectional dc–dc converter, soft switching and bidirectional power conversion can be achieved with some control strategies [17]–[21]. However, these converters are controlled

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to operate in a forward operation mode or backward operation mode, respectively. As load current of class-D audio amplifier varies rapidly and randomly, which makes it difficult to realize soft switching by detecting the direction of the load current. Thus, these bidirectional soft switching dc–dc converters are not suitable for the class-D audio amplifier system.

As a good candidate for the front-end dc–dc converter, *LLC* resonant converter attracts much attention in decades. There are many research works on the control, common noise, and magnetics design of *LLC* converter [22]–[26]. However, due to the complex control algorithm, these converters require a microcontroller to achieve start-up and other control functions. In a bidirectional soft switching *LLC* dc–dc converter, some control strategies and circuit topologies are designed for soft switching of all the switches in forward or backward mode as well as smooth change of the output power flow direction [27]–[29]. Because maximum output frequency of audio amplifier is 20 kHz, it is difficult to design the controller of bidirectional *LLC* converter for the audio amplifier system.

In a class-D audio amplifier system, because the downstream class-D audio amplifier is close-loop and always has high PSRR, the front-end dc–dc converter can be designed as an open-loop dc-transformer (DCX) to improve the efficiency and reduce the complexity of the controller. Light load efficiency and an optimized magnetic component of the *LLC* DCX are the focus in [30]–[35]. A family of resonant DCX is proposed in [36], which achieve soft switching of switches and high system efficiency over wide load range. However, it is difficult to realize soft switching of all the switches in both forward and backward mode because these DCXs are open-loop and has fixed switching frequency as well as fixed duty cycle.

In this paper, a soft switching symmetric bipolar outputs DCX for eliminating power supply pumping of the half-bridge class-D audio amplifier is proposed. Power supply pumping of the half-bridge class-D audio amplifier is eliminated by the proposed DCX with small output capacitances, thus power supply noise and voltage stress of the devices in the half-bridge class-D audio amplifier are reduced. The proposed DCX has stable symmetric bipolar outputs with the simple open-loop controller, which significantly reduces the complexity of controller in the half-bridge class-D audio amplifier system. Soft switching of the switches in the proposed DCX can be realized when the load current of the half-bridge class-D audio amplifier is positive or negative, which improves the system efficiency.

This paper is organized as follows. Section II discusses power supply pumping and the circuit configuration of the proposed DCX. Section III contains the analysis of operation modes and performance of the proposed DCX. Sections V and VI contain experimental results and conclusion.

## II. Power Supply Pumping and Topology Derivation of the Proposed DCX

The proposed audio amplifier system, as shown in Fig. 1, consists of front-end DCX and downstream class-D audio amplifier. The proposed DCX has bidirectional power flowing path. Thus, the power supply pumping of the half-bridge class-D amplifier

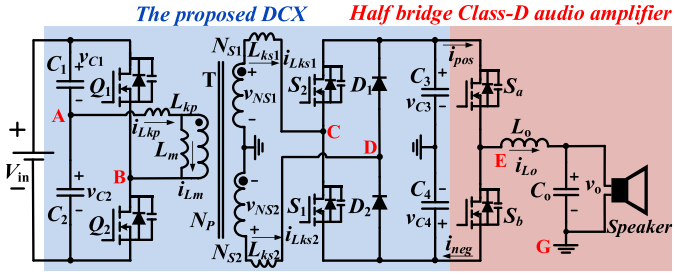


Fig. 1. Circuit diagram of the proposed audio amplifier system.

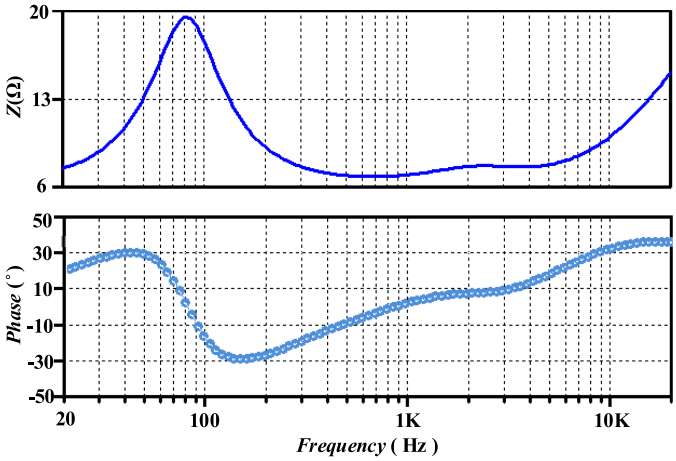


Fig. 2. Typical impedance of speaker versus different output voltage frequency of the audio amplifier.

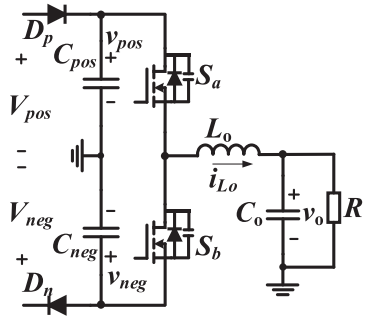

Fig. 3. Half-bridge class-D audio amplifier with a unidirectional front-end dc–dc converter.

can be reduced since a current path is provided for the reverse load current.

### A. Power Supply Pumping of Half-Bridge Class-D Amplifier

Fig. 2 shows the impedance of the speaker versus the output voltage frequency of an audio amplifier. It can be observed that speaker load can be resistive, capacitive, or inductive under different output voltage frequency.

Fig. 3 shows the half-bridge class-D audio amplifier with a unidirectional front-end dc–dc converter, and the load is assumed as a resistor. Due to unidirectional power flowing paths, the reverse load current would cause output voltage pumping of the front-end dc–dc converter. Such voltages pumping

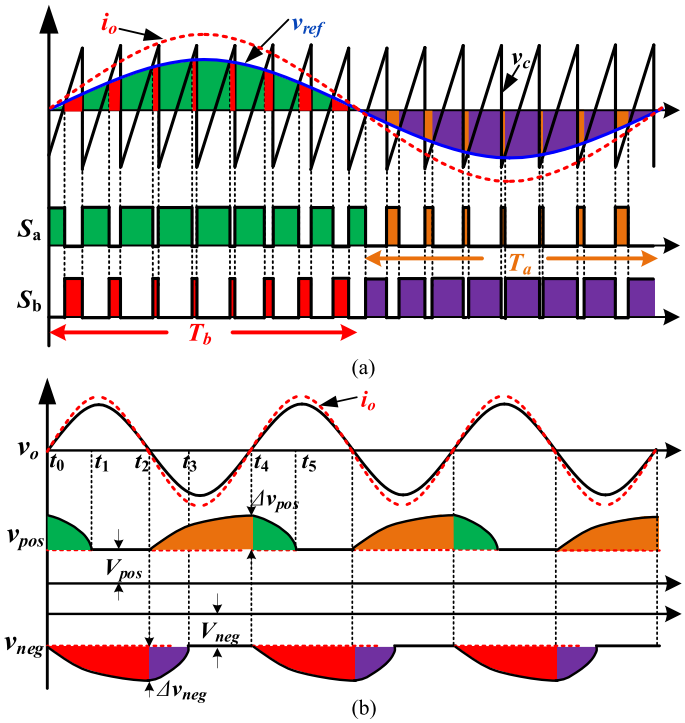


Fig. 4. Power supply pumping of half-bridge class-D audio amplifier with a unidirectional front-end dc–dc converter under resistor load. (a) Key waveforms of the half-bridge class-D audio amplifier. (b) Power supply pumping of the half-bridge class-D audio amplifier system.

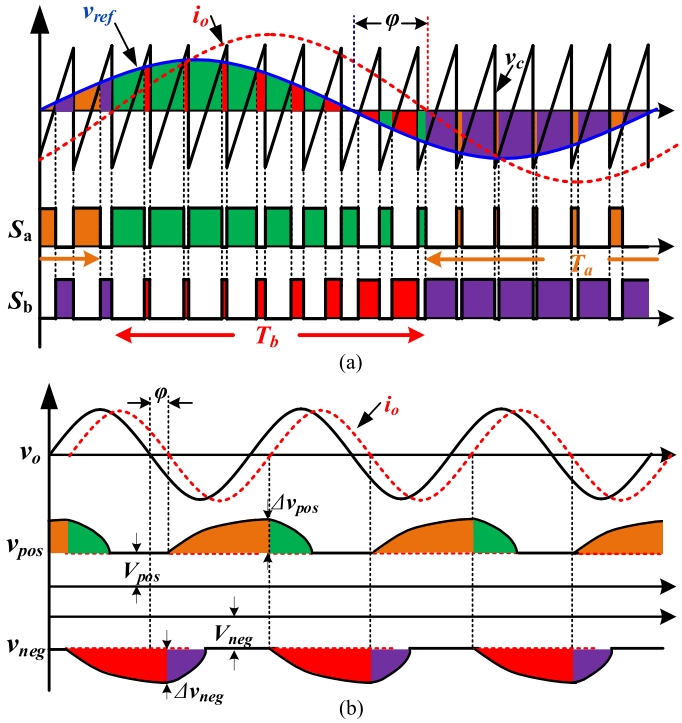


Fig. 5. Power supply pumping of the half-bridge class-D audio amplifier with a unidirectional front-end dc–dc converter under inductive load. (a) Key waveforms of the half-bridge class-D audio amplifier. (b) Power supply pumping of the half-bridge class-D audio amplifier system.

increases voltage stress of switches $S_a$, $S_b$ as well as capacitors $C_{\text{pos}}, C_{\text{neg}}$, and deteriorates the power supply noise of the half-bridge class-D audio amplifier.

Fig. 4 illustrates the power supply pumping of the half-bridge class-D audio amplifier system as shown in Fig. 3 with resistor load. In Fig. 4(a), $i_o$ is load current of the half-bridge class-D audio amplifier, $v_{\text{ref}}$ is audio reference voltage, and $v_c$ is carrier. The driving signals of switches $S_a$ and $S_b$ are complementary, $T_a$ is the time when load current is negative and $T_b$ is the time when load current is positive.

For negative load current $i_o$, when switch $S_a$ is turned ON and switch $S_b$ is turned OFF, load current $i_o$ flows from filter inductor $L_o$ into capacitor $C_{\text{pos}}$ through switch $S_a$. Thus, the charge is stored in capacitor $C_{\text{pos}}$, which causes bus pumping on positive power supply of the class-D audio amplifier. Because voltage $v_{\text{pos}}$ is higher than positive power supply voltage $V_{\text{pos}}$, diode $D_p$ is turned OFF. When switch $S_b$ is turned ON and switch $S_a$ is turned OFF, load current $i_o$ flows from filter inductor $L_o$ into diode $D_n$ through switch $S_b$. Thus, the negative power supply of the class-D audio amplifier provides power for the load.

For positive load current $i_o$, when switch $S_b$ is turned ON and switch $S_a$ is turned OFF, load current $i_o$ flows from switch $S_b$ into filter inductor $L_o$. Thus, the charge is stored in capacitor $C_{\text{neg}}$, which causes bus pumping on negative power supply of the class-D audio amplifier. Because voltage $v_{\text{neg}}$ is lower than negative power supply voltage $V_{\text{neg}}$, diode $D_n$ is turned OFF. When switch $S_a$ is turned ON and switch $S_b$ is turned OFF, load current $i_o$ flows from diode $D_p$ into filter inductor $L_o$ through switch $S_a$. Thus, the positive power supply of the class-D audio amplifier provides power for the load.

As shown in Fig. 4(a), yellow area represents the time when load current $i_o$ is negative and flows into capacitor $C_{\text{pos}}$ through switch $S_a$. Red area represents the time when load current $i_o$ is positive and flows into $C_{\text{neg}}$ through switch $S_b$. Green and purple areas represent the time when positive and negative power supply provide output power for the load through switches $S_a$ and $S_b$, respectively. It can be observed that the time of green area is longer than the time of yellow area and the time of purple area is longer than the time of red area.

In Fig. 4(b), $V_{\text{pos}}$ and $V_{\text{neg}}$ are positive and negative bus voltage for class-D audio amplifier, and $\Delta v_{\text{pos}}$ and $\Delta v_{\text{neg}}$ are positive and negative bus pumping voltage. As shown in Fig. 4(b), when load current $i_o$ is positive and switch $S_a$ is turned ON, the charge stored in capacitor $C_{\text{pos}}$ is discharged to provide output power for the load. Thus, during the time interval $t_4$–$t_5$, voltage $v_{\text{pos}}$ decreases from the maximum to positive bus voltage $V_{\text{pos}}$. When load current $i_o$ is negative and switch $S_b$ is turned ON, the charge stored in capacitor $C_{\text{neg}}$ is discharged to provide output power for the load. Thus, during the time interval $t_2$–$t_3$, voltage $v_{\text{neg}}$ increases from the minimum to negative bus voltage $V_{\text{neg}}$.

When the speaker load of the audio amplifier is inductive or capacitive, load current $i_o$ in Fig. 4(a) will shift to the right or left. Fig. 5 illustrates the power supply pumping of the half-bridge class-D audio amplifier system as shown in Fig. 3 with an inductive load. With inductive or capacitive load, when load current $i_o$ is negative and switch $S_a$ is turned ON, the time of yellow area is longer than that with resistive load, which

causes more severe bus pumping on capacitor $C_{\text{pos}}$. Similarly, when load current $i_o$ is positive and switch $S_b$ is turned ON, the time of red area is longer than that with resistive load, which causes more severe bus pumping on capacitor $C_{\text{neg}}$. The analysis of power supply pumping of the half-bridge class-D audio amplifier system with inductive load is similar to that with resistive load.

In order to calculate the power supply pumping of the half-bridge class-D audio amplifier, setting

$$\begin{cases} v_o = mV_{\text{bus}}\sin(\omega t) \\ i_o = \frac{mV_{\text{bus}}\sin(\omega t+\varphi)}{|Z_{\text{speaker}}|} \end{cases} \tag{1}$$

where $m$ is modulation index of class-D audio amplifier, $V_{\text{bus}}$ is power supply voltage of the class-D audio amplifier, which equals to the magnitude of $V_{\text{pos}}$ and $V_{\text{neg}}$, $\omega$ is angular frequency of output voltage of audio amplifier, $\varphi$ is phase difference which the output current lags output voltage of audio amplifier, and $Z_{\text{speaker}}$ is impedance of the speaker.

In the half-bridge class-D audio amplifier, the duty cycle of switch $S_a$ is as follows:

$$d_{Sa} = \frac{1}{2} + \frac{1}{2}m\sin(\omega t). \tag{2}$$

As shown in Fig. 5, during $T_a$, load current $i_o$ flows into capacitor $C_{\text{pos}}$ through switch $S_a$, which increases the voltage across capacitor $C_{\text{pos}}$. If switching frequency and output voltage frequency of the class-D audio amplifier satisfy $f_s : f_o = N$, the voltage ripple across positive power supply $\Delta v_{\text{pos}}$ satisfy

$$\begin{aligned} C_{\text{pos}}\cdot\Delta v_{\text{pos}} &= \int_{\frac{\pi-\varphi}{\omega}}^{\frac{2\pi-\varphi}{\omega}} -i_{Sa}(t)dt \\ &= \sum_{i=N/2}^{N}\left\{-\frac{mV_{\text{pos}}}{|Z_{\text{speaker}}|}\sin\left(\frac{\omega i}{N}+\varphi\right)\right. \\ &\quad \left.\cdot\left[\frac{1}{2}+\frac{1}{2}m\sin\left(\frac{\omega i}{N}\right)\right]\right\}. \end{aligned} \tag{3}$$

When $N \to +\infty$, (3) can be rewritten as follows:

$$\begin{aligned} C_{\text{pos}}\cdot\Delta v_{\text{pos}} &= \int_{\pi}^{2\pi} -\frac{mV_{\text{pos}}}{\omega\,|Z_{\text{speaker}}|}\sin(x) \\ &\quad \times\left[\frac{1}{2}+\frac{1}{2}m\sin(x-\varphi)\right]dx \\ &= \frac{mV_{\text{pos}}(4-m\pi\cos\varphi)}{4\omega\,|Z_{\text{speaker}}|}. \end{aligned} \tag{4}$$

Therefore, the ripple voltage across positive power supply is as follows:

$$\Delta v_{\text{pos}} = \frac{mV_{\text{pos}}(4-m\pi\cos\varphi)}{8\pi f_o\,|Z_{\text{speaker}}|\,C_{\text{pos}}}. \tag{5}$$

Similarly, the ripple voltage across negative power supply is as follows:

$$\Delta v_{\text{neg}} = \frac{mV_{\text{pos}}(4-m\pi\cos\varphi)}{8\pi f_o\,|Z_{\text{speaker}}|\,C_{\text{neg}}}. \tag{6}$$

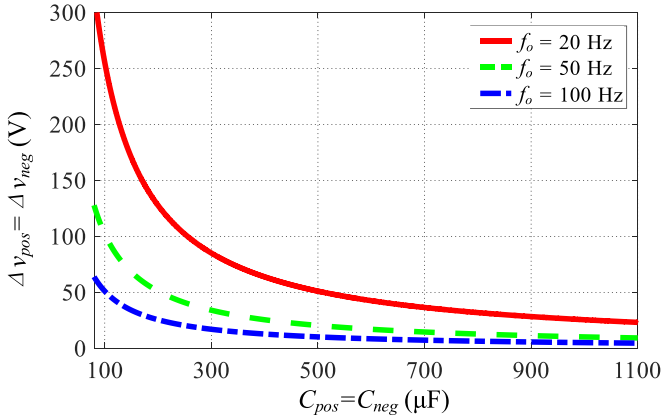


Fig. 6. Voltage ripple $\Delta v_{\text{pos}} = \Delta v_{\text{neg}}$ versus capacitances $C_{\text{pos}} = C_{\text{neg}}$.

It can be observed from (5) and (6) that when output voltage frequency of audio amplifier is low, power supply pumping is severe. Assume that $m = 0.7$, $V_{\text{pos}} = 35$ V, $Z_{\text{load}} = 4\ \Omega$ and $\varphi = \pi/6$, according to (5) and (6), Fig. 6 shows the relationship between $\Delta v_{\text{pos}} = \Delta v_{\text{neg}}$ and capacitances $C_{\text{pos}} = C_{\text{neg}}$. As shown in Fig. 6, if $f_o = 20$ Hz, $\Delta v_{\text{pos}} = \Delta v_{\text{neg}} = 35$ V, large capacitors $C_{\text{pos}} = C_{\text{neg}} = 731.1\ \mu$F with 70 V voltage stress are needed. If smaller voltage ripple $\Delta v_{\text{pos}} = \Delta v_{\text{neg}}$ is required, it has to increase capacitances $C_{\text{pos}} = C_{\text{neg}}$, which reduces power density of the audio amplifier system.

If the diodes $D_p$ and $D_n$ in Fig. 3 are replaced by switches and bidirectional current flowing path is provided for the half-bridge class-D audio amplifier, the charge can be transferred instead of stored in the capacitors $C_{\text{pos}}$ and $C_{\text{neg}}$, thus power supply pumping can be eliminated.

### *B. Topology Derivation of the Proposed DCX*

Half-bridge circuit, full-bridge circuit, push-pull circuit, two-switch forward circuit, etc., can be used in transformer primary to generate square wave voltage with 0.5 duty cycle. Fig. 7 shows the circuit configuration of the proposed DCX. When square wave with a constant duty cycle is generated in the transformer primary, the proposed DCX can generate constant positive and negative output voltages when a full-wave or full-bridge rectifier is adopted in transformer secondary. Thus, if the leakage inductance of the transformer is neglected, the bipolar output voltages of the proposed DCX are always clamped by the input voltage of the DCX. Therefore, the voltage ripples across outputs of the proposed DCX are theoretically zero, even if output capacitors of the DCX are zero. Thus, the output filter of the DCX is reduced, and the power density of the proposed audio amplifier system can be improved.

In Fig. 7, in order to generate symmetric bipolar outputs, two full-bridge rectifiers are necessary to ensure constant output voltages in type I DCX, as shown in Fig. 7(a). Compared with type II DCX as shown in Fig. 7(b), type I DCX needs more rectifier diodes or switches. Thus, type II DCX with half-bridge circuit in the transformer primary is adopted.

Fig. 8 shows four kinds of the rectifier. Front-end bidirectional dc–dc converter is required to reduce power supply pumping in

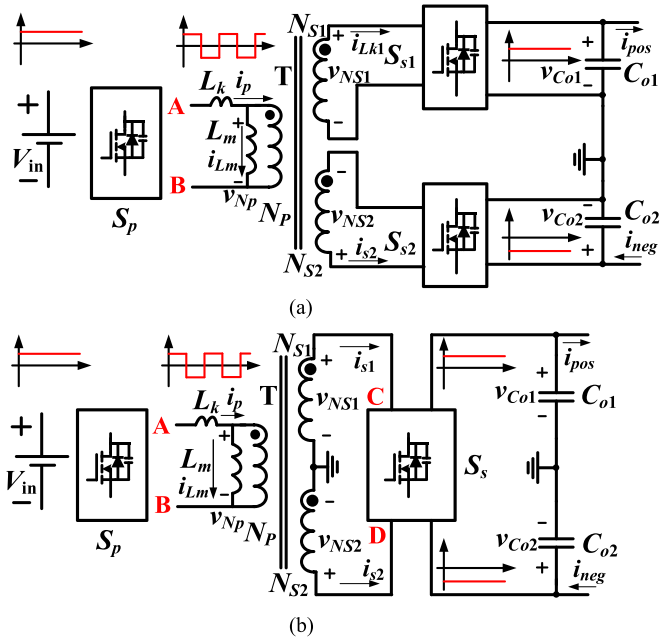


Fig. 7. Circuit configuration of the proposed DCX. (a) Type I. (b) Type II.

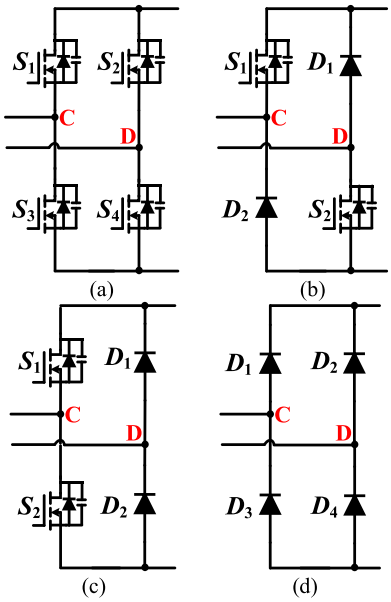


Fig. 8. Circuit diagram of rectifier.

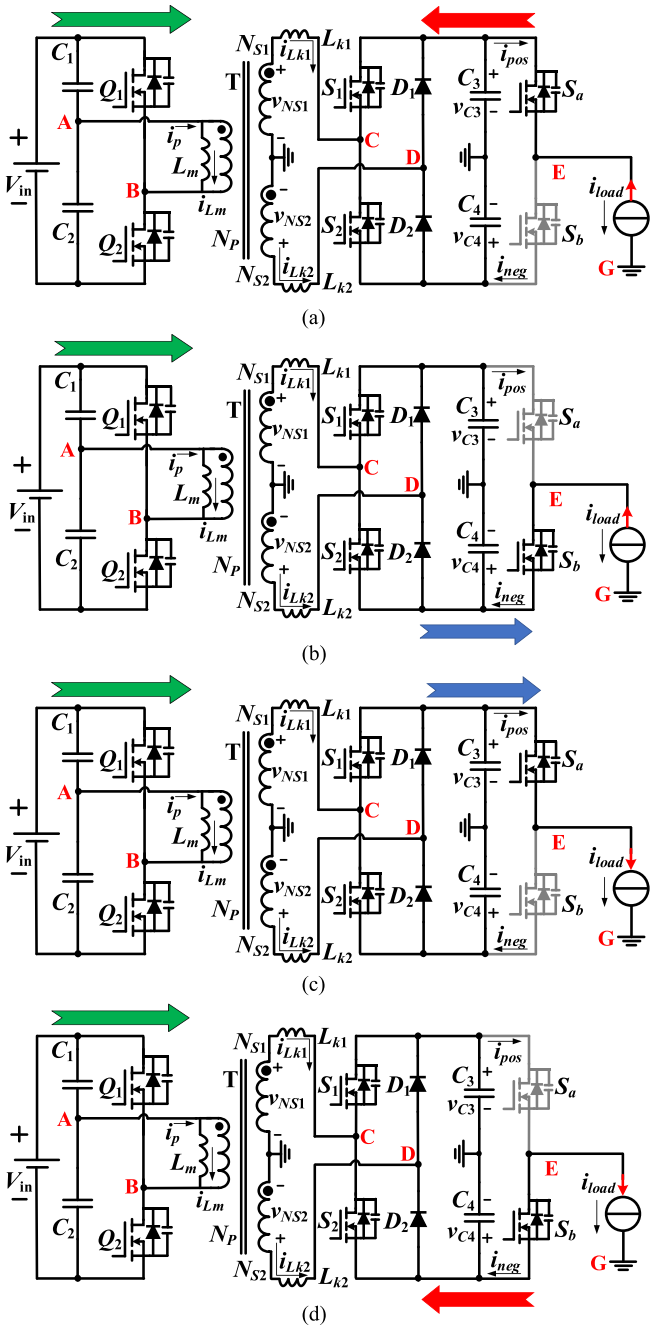


Fig. 9. Circuit diagram of power flow in the proposed DCX. (a) Negative load current of the class-D audio amplifier when switch $S_a$ is turned ON. (b) Negative load current of the class-D audio amplifier when switch $S_b$ is turned ON. (c) Positive load current of class-D audio amplifier when switch $S_a$ is turned ON. (d) Positive load current of class-D audio amplifier when switch $S_b$ is turned ON.

the half-bridge class-D audio amplifier and provide a path for the reserve load current. The rectifier as shown in Fig. 8(c) is adopted in the proposed DCX due to bidirectional power conversion with less active devices.

## III. Analysis of Operation Modes and Characteristic of the Proposed DCX

In this paper, the proposed DCX is connected to the half-bridge class-D audio amplifier. For an audio amplifier, the load current is ac and the frequency range of load current is 20 Hz–20 kHz, which is much lower than the switching frequency of the proposed DCX. Therefore, in one switching period of the proposed DCX, the load current of the half-bridge class-D audio amplifier can be regarded as constant since filter inductor is large and ripple current of filter inductor is small.

Fig. 9 shows the circuit diagram of power flow in the proposed DCX. As shown in Fig. 9(a), for negative load current, when switch $S_a$ is turned ON, current $i_{\text{load}}$ flows from switch $S_a$ to

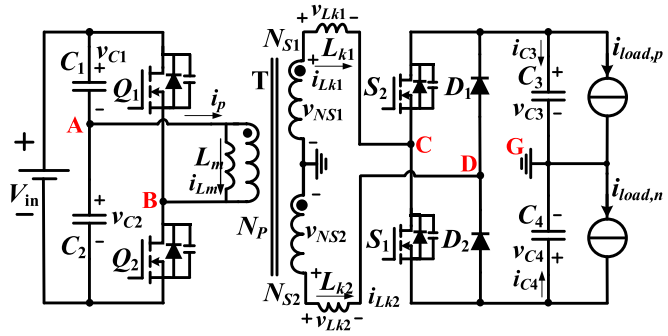


Fig. 10. Equivalent circuit of the proposed DCX.

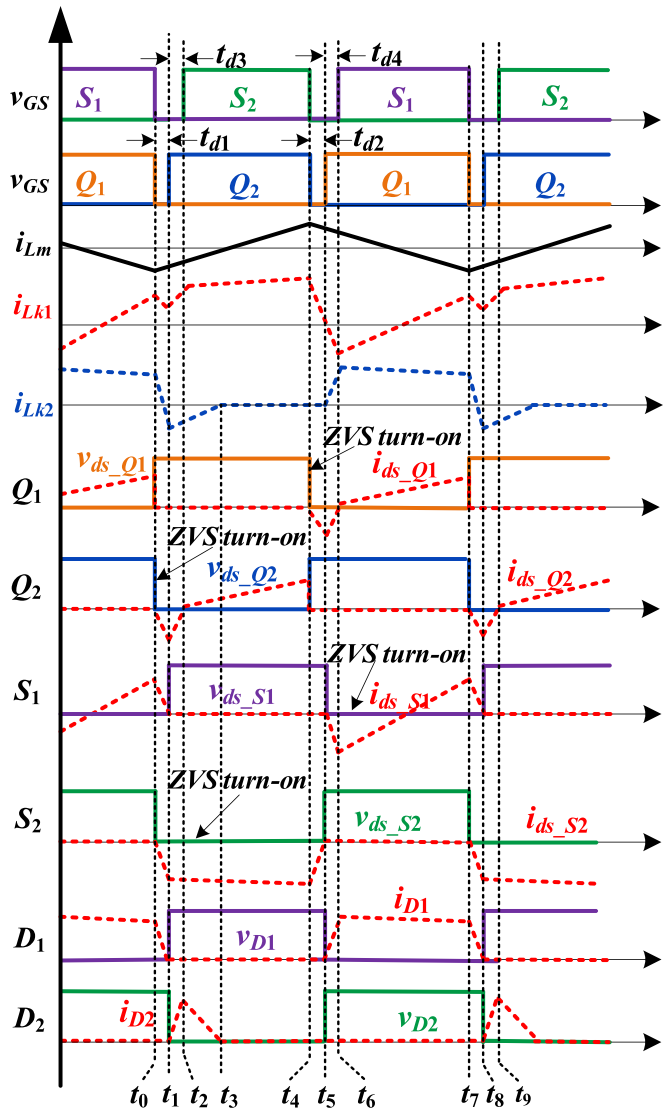


Fig. 11. Key waveforms of the proposed DCX when currents $i_{\text{load},p} > 0$ and $i_{\text{load},n} < 0$.

capacitor $C_3$ and positive bus is charged. Therefore, the power is returned to positive bus. As shown in Fig. 9(b), for negative load current, when switch $S_b$ is turned ON, current $i_{\text{load}}$ flows from switch $S_b$ to capacitor $C_4$. Therefore, the power is consumed by the load. As shown in Fig. 9(c), for positive load current, when switch $S_a$ is turned ON, current $i_{\text{load}}$ flows from capacitor $C_3$ to switch $S_a$. Therefore, the power is consumed by the load. As shown in Fig. 9(d), for positive load current, when switch $S_b$ is turned ON, current $i_{\text{load}}$ flows from capacitor $C_4$ to switch $S_b$ and negative bus is discharged. Therefore, the power is returned to negative bus.

As shown in Fig. 5(a), if $-90° < \varphi < 90°$, the time of green area is longer than the time of yellow area, and the time of purple area is longer than the time of red area, which means that the conduction time of switch $S_b$ is longer than that of switch $S_a$ when current $i_{\text{load}}$ is negative, and the conduction time of switch $S_a$ is longer than that of switch $S_b$ when current $i_{\text{load}}$ is positive. Thus, the average power of the proposed DCX is positive when the load current is positive or negative. In the proposed DCX, positive and negative outputs have bidirectional power, input port has unidirectional power. For positive output, the feedback energy can be consumed by the negative output, and for negative output, the feedback energy can be consumed by the positive output.

In order to ensure low-distortion of the output voltage at 20 kHz or even higher audio signal frequency, the switching frequency of class-D audio amplifier is generally very high. As the switching frequency of class-D audio amplifier is higher than the switching frequency of the proposed DCX, when the operation mode of the proposed DCX is analyzed, the load current can be regarded as two average equivalent current sources for the positive and negative bus. The average equivalent current sources $i_{\text{load},p}$ and $i_{\text{load},n}$ satisfy

$$\begin{cases} i_{\text{load},p}(t) = d_{Sa} i_{\text{load}} = d_{Sa} i_o \\ i_{\text{load},n}(t) = d_{Sb} i_{\text{load}} = d_{Sb} i_o. \end{cases} \tag{7}$$

From (1), (2), and (7), average equivalent current sources $i_{\text{load},p}$ and $i_{\text{load},n}$ are as follows:

$$\begin{cases} i_{\text{load},p}(t) = \left[\frac{1}{2} + \frac{1}{2} m \sin(\omega t)\right] \frac{m V_{\text{bus}} \sin(\omega t + \varphi)}{|Z_{\text{speaker}}|} \\ i_{\text{load},n}(t) = -\left[\frac{1}{2} - \frac{1}{2} m \sin(\omega t)\right] \frac{m V_{\text{bus}} \sin(\omega t + \varphi)}{|Z_{\text{speaker}}|}. \end{cases} \tag{8}$$

In order to simplify the analysis of the proposed DCX as shown in Fig. 2, assume that all power switches are ideal except their body diode and output capacitances $C_{\text{oss}}$, the output capacitances of all switches are the same, and the diodes are ideal. Fig. 10 shows the equivalent circuit of the proposed DCX connected half-bridge class-D audio amplifier.

### *A. Operation Modes of the Proposed DCX When Load Current of Class-D Audio Amplifier is Positive*

When load current of the half-bridge class-D audio amplifier is positive, currents $i_{\text{load},p}$ and $i_{\text{load},n}$ satisfy $i_{\text{load},p} > 0$ and $i_{\text{load},n} < 0$ in the equivalent circuit of the proposed DCX. Fig. 11 shows the key waveforms of the proposed DCX. As shown in Fig. 11, $t_{d1}$ and $t_{d2}$ are the dead time of primary side half-bridge circuit. If $t_{d1}$ and $t_{d2}$ are neglected, the driving signals of switches $Q1$ and $Q2$ are complementary with constant duty cycle 0.5. In order to ensure soft switching of switches $S1$–$S2$, the turn-ON of switches $S1$ and $S2$ should lag behind the turn-ON of switch $Q1$ and $Q_2$ with a delay time $t_{d3}$ and $t_{d4}$. If dead time and delay time are neglected, the driving signals of switches

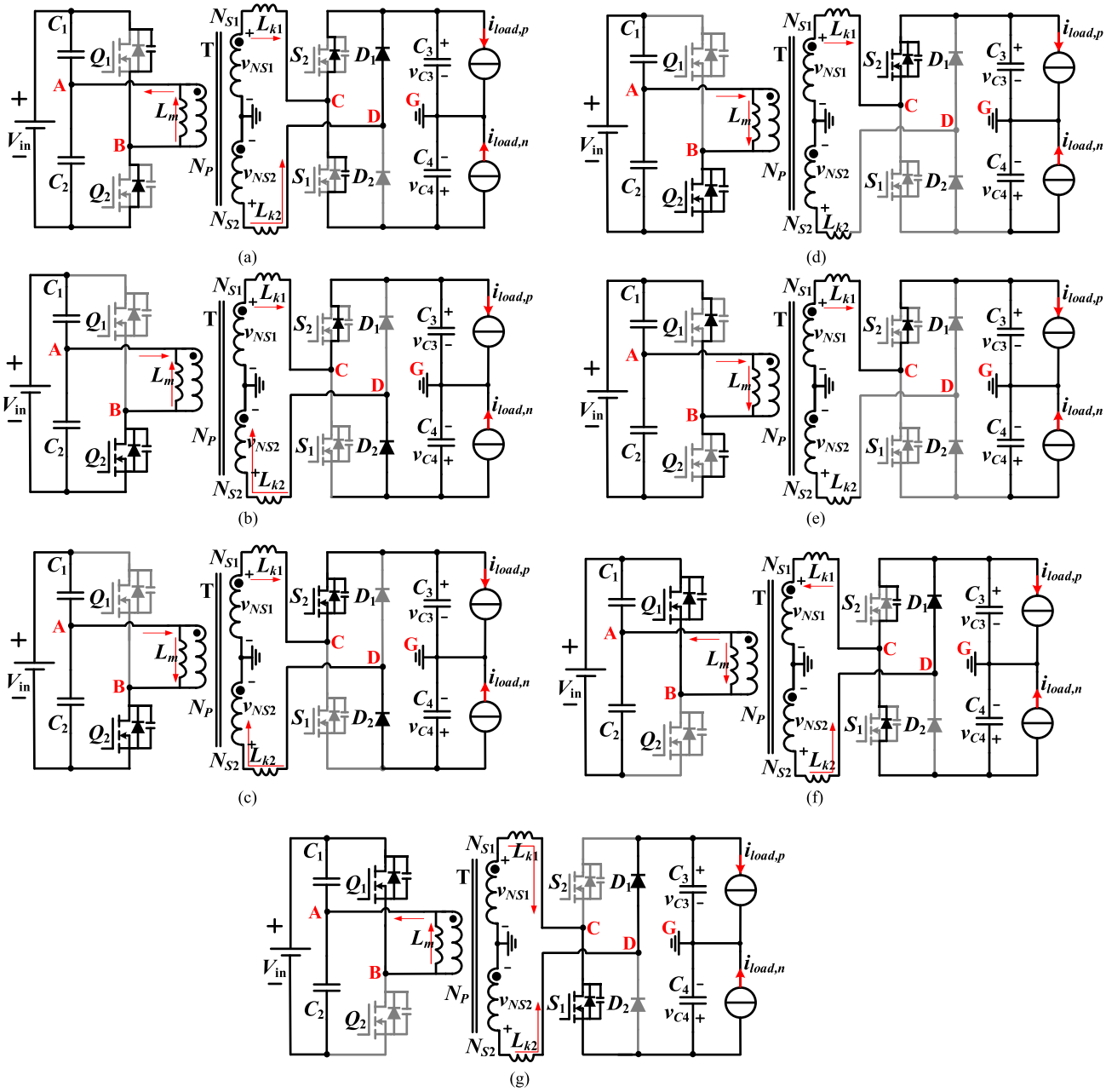


Fig. 12. Operation mode of the proposed DCX when currents $i_{\text{load},p} > 0$ and $i_{\text{load},n} < 0$. (a) Mode 1$(t_0$–$t_1)$. (b) Mode 2$(t_1$–$t_2)$. (c) Mode 3 $(t_2$–$t_3)$. (d) Mode 4 $(t_3$–$t_4)$. (e) Mode 5 $(t_4$–$t_5)$. (f) Mode 6 $(t_5$–$t_6)$. (g) Mode 7 $(t_6$–$t_7)$.

$S1$ and $S2$ are complementary with constant duty cycle 0.5. In steady state, the proposed DCX has seven operation modes as shown in Fig. 12.

*Mode 1 [$t_0$–$t_1$]:* At $t_0$, switches $Q_1$ and $S_1$ are turned OFF, the proposed DCX operates in dead time mode. After switches $Q_1$ and $S_1$ are turned OFF, the output capacitor of switch $Q_1$ is charged and the output capacitor of switch $Q_2$ is discharged. Voltage across node A and node B $v_{\text{AB}}$ changes from negative to positive, thus current $i_{LK2}$ decreases. The body diode of switch $S_2$ is conducted to provide current flowing paths for the free-wheeling of secondary leakage inductance current $i_{LK1}$. When the output capacitor of switch $Q_2$ is completely discharged, the body diode of switch $Q_2$ is conducted and ZVS turn-ON of switch $Q_2$ can be achieved. This mode is short and ends when switch $Q_2$ is turned ON at $t_1$.

To ensure ZVS turn-ON of switch $Q_2$, it should have

$$\frac{1}{2}\frac{L_{k1}+L_{k2}}{4n^2}[-ni_{Lk1}(t_0)+ni_{Lk2}(t_0)-i_{Lm}(t_0)]^2 + \frac{1}{2}L_m i_{Lm}(t_0)^2 > \frac{1}{2}(C_{\text{oss},Q1}+C_{\text{oss},Q2}){V_{\text{in}}}^2. \quad (9)$$

It can be observed from (9), $L_m$ is much larger than $L_{k1}$ and $L_{k2}$, and ZVS turn-ON of switch $Q_2$ can be achieved easily. If ZVS turn-ON of switch $Q_2$ can be achieved in dead time

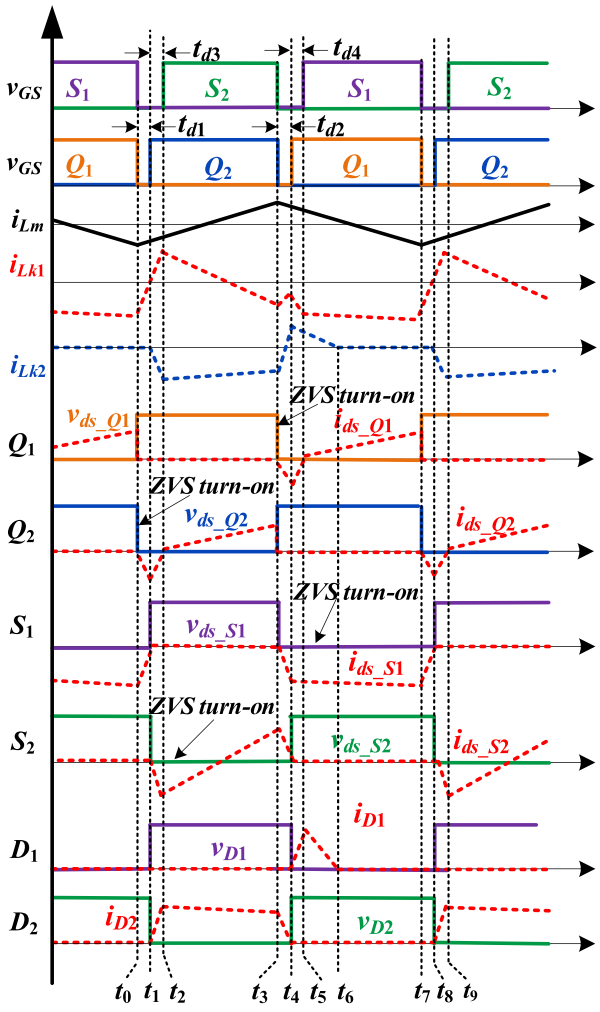


Fig. 13 Key waveforms of the proposed DCX when currents $i_{\text{load},p} < 0$ and $i_{\text{load},n} > 0$.

$t_{d1}, t_{d1} = t_1 - t_0$ should satisfy

$$\int_{t_0}^{t_1} [-ni_{Lk1} + ni_{Lk2} - i_{Lm}]dt > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \tag{10}$$

Because current $i_{Lm}$ can be regarded as constant during $t_{d1}$, (10) can be approximated and rewritten as follows:

$$-i_{Lm}(t_0)t_{d1} = \frac{V_{\text{in}}T}{4L_m}t_{d1} > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \tag{11}$$

*Mode 2 [$t_1$–$t_2$]:* At $t_1$, switch $Q_2$ is turned ON, and the proposed DCX operates in delay time mode. In this mode, because voltage $v_{\text{AB}}$ is positive, current $i_{LK1}$ is positive and current $i_{LK2}$ is negative, the body diode of $S_2$ and diode $D_2$ are conducted to provide current flowing paths for currents $i_{LK1}$ and $i_{LK2}$. This mode is short and ends when switch $S_2$ is turned ON at $t_2$.

*Mode 3 [$t_2$–$t_3$]:* At $t_2$, switch $S_2$ achieves ZVS turn-ON. In this mode, because the load current $i_{\text{load},p}$ is positive and the load current $i_{\text{load},n}$ is negative, the input power supply provides power for positive output through leakage inductance $L_{k1}$ and switch $S_2$.

In this mode, because the load current $i_{\text{load},n}$ is negative, voltage $v_{C4}$ decreases and is lower than $v_{NS2}$. Current $i_{LK2}$ increases from negative to zero, and diode $D_2$ achieves ZCS turn-OFF. This mode ends when diode $D_2$ is turned OFF at $t_3$.

*Mode 4 [$t_3$–$t_4$]:* At $t_3$, diode $D_2$ is turned OFF. In this mode, switches $Q_2$ and $S_2$ are conducted. Current $i_{LK1}$ still flows from switch $S_2$ to capacitor $C_3$. This mode ends when switches $Q_2$ and $S_2$ are turned OFF at $t_4$.

*Mode 5 [$t_4$–$t_5$]:* At $t_4$, switches $Q_2$ and $S_2$ are turned OFF. The proposed DCX operates in dead time mode. After switches $Q_2$ and $S_2$ are turned OFF, the output capacitor of switch $Q_2$ is charged and the output capacitor of switch $Q_1$ is discharged. Voltage across node A and node B $v_{\text{AB}}$ changes from positive to negative, thus current $i_{LK1}$ decreases sharply. The body diode of switch $S_2$ is still conducted when current $i_{LK1}$ is positive. When the output capacitor of switch $Q_1$ is completely discharged, the body diode of switch $Q_1$ is conducted and ZVS turn-ON of switch $Q_1$ can be achieved. This mode is short and ends when switch $Q_1$ is turned ON at $t_1$.

To ensure ZVS turn-ON of switch $Q_1$, it should have

$$\frac{1}{2}\frac{L_{k1} + L_{k2}}{4n^2}[ni_{Lk1}(t_4) + i_{Lm}(t_4)]^2 + \frac{1}{2}L_m i_{Lm}(t_4)^2 > \frac{1}{2}(C_{\text{oss},Q1} + C_{\text{oss},Q2}){V_{\text{in}}}^2. \tag{12}$$

It can be observed from (12), $L_m$ is much larger than $L_{k1}$ and $L_{k2}$, and ZVS turn-ON of switch $Q_1$ can be achieved easily. If ZVS turn-ON of switch $Q_1$ can be achieved in dead time $t_{d2}, t_{d2} = t_5 - t_4$ should satisfy

$$\int_{t_4}^{t_5} [ni_{Lk1} + i_{Lm}]dt > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \tag{13}$$

Because current $i_{Lm}$ can be regard as constant during $t_{d2}$, (13) can be approximated and rewritten as follows:

$$i_{Lm}(t_4)t_{d2} = \frac{V_{\text{in}}T}{4L_m}t_{d2} > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \tag{14}$$

*Mode 6 [$t_5$–$t_6$]:* At $t_5$, switch $Q_1$ is turned ON, and the proposed DCX operates in delay time mode. Current $i_{LK1}$ decreases to negative and current $i_{LK2}$ is positive. In this mode, the body diode of $S_1$ and diode $D_1$ are conducted to provide current flowing paths for currents $i_{LK1}$ and $i_{LK2}$. This mode is short and ends when switch $S_1$ is turned ON at $t_6$.

*Mode 7 [$t_6$–$t_7$]:* At $t_6$, switch $S_1$ achieves ZVS turn-ON. Because the load current $i_{\text{load},p}$ is positive and the load current $i_{\text{load},n}$ is negative. In this mode, the input power supply provides power for positive output through leakage inductance $L_{k2}$ and diode $D_1$.

Because the load current $i_{\text{load},n}$ is negative and capacitor $C_4$ is discharged in mode 3 as shown in Fig. 12, current $i_{LK1}$ increases from negative to positive and flows form switch $S_1$ to capacitor $C_4$ to balance the charge of capacitor $C_4$ in this mode. This mode ends when switches $Q_1$ and $S_1$ are turned OFF at $t_7$.

### *B. Operation Modes of the Proposed DCX When Load Current of Class-D Audio Amplifier is Negative*

When load current of the half-bridge class-D audio amplifier is negative, currents $i_{\text{load},p}$ and $i_{\text{load},n}$ satisfy $i_{\text{load},p} < 0$ and $i_{\text{load},n} > 0$ in the equivalent circuit of the proposed DCX. Fig. 13 shows the key waveforms of the proposed DCX. As shown in

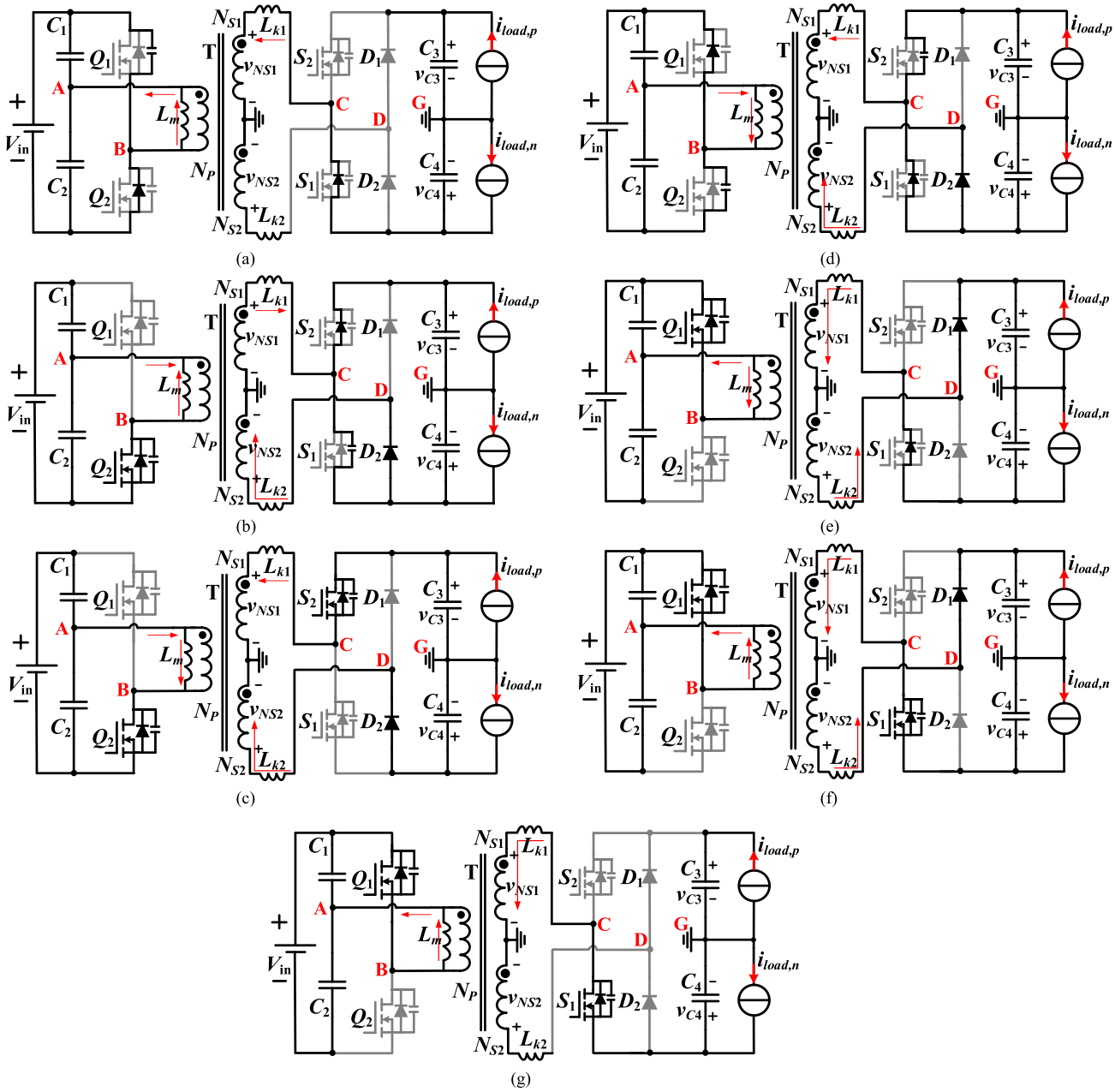


Fig. 14. Operation mode of the proposed DCX. (a) Mode 1 ($t_0$–$t_1$). (b) Mode 2 ($t_1$–$t_2$). (c) Mode 3 ($t_2$–$t_3$). (d) Mode 4 ($t_3$–$t_4$). (e) Mode 5 ($t_4$–$t_5$). (f) Mode 6 ($t_5$–$t_6$). (g) Mode 7 ($t_6$–$t_7$).

Fig. 13, $t_{d1}$ and $t_{d2}$ are the dead time of the primary side half-bridge circuit. If $t_{d1}$ and $t_{d2}$ are neglected, the driving signals of switches $Q1$ and $Q2$ are complementary with constant duty cycle 0.5. In order to ensure soft switching of switches $S1-S2$, the turn-ON of switches $S1$ and $S2$ lags behind the turn-ON of switch $Q1$ and $Q_2$ with a delay time $t_{d3}$ and $t_{d4}$. If $t_{d3}$ and $t_{d4}$ are neglected, the driving signals of switches $S1$ and $S2$ are complementary with constant duty cycle 0.5. In steady state, the proposed DCX has seven operation modes as shown in Fig. 14.

*Mode 1 [$t_0$–$t_1$]:* At $t_0$, switches $Q_1$ and $S_1$ are turned OFF, the proposed DCX operates in dead time mode. After switches $Q_1$ and $S_1$ are turned OFF, the output capacitor of switch $Q_1$ is charged and the output capacitor of switch $Q_2$ is discharged. Voltage across node A and node B $v_{AB}$ changes from negative to positive, thus current $i_{LK1}$ increases sharply. The body diode of switch $S_1$ is still conducted when current $i_{LK1}$ is negative. When the output capacitor of switch $Q_2$ is completely discharged, the body diode of switch $Q_2$ is conducted and ZVS turn-ON of switch $Q_2$ can be achieved. This mode is short and ends when switch $Q_2$ is turned ON at $t_1$.

To ensure ZVS turn-ON of switch $Q_2$, it should have

$$\frac{1}{2}\frac{L_{k1}+L_{k2}}{4n^2}[-ni_{Lk1}(t_0)-i_{Lm}(t_0)]^2+\frac{1}{2}L_m i_{Lm}(t_0)^2 > \frac{1}{2}(C_{\text{oss},Q1}+C_{\text{oss},Q2}){V_{\text{in}}}^2. \quad (15)$$

It can be observed from (15), $L_m$ is much larger than $L_{k1}$ and $L_{k2}$, and ZVS turn-ON of switch $Q_1$ can be achieved easily. If ZVS turn-ON of switch $Q_1$ can be achieved in dead time $t_{d1}, t_{d1} = t_1 - t_0$ should satisfy

$$\int_{t_0}^{t_1} [-ni_{Lk1} - i_{Lm}]dt > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \quad (16)$$

Because current $i_{Lm}$ can be regard as constant during $t_{d1}$, (16) can be approximated and rewritten as follows:

$$-i_{Lm}(t_0)t_{d1} = \frac{V_{\text{in}}T}{4L_m}t_{d1} > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \quad (17)$$

*Mode 2 [$t_1$–$t_2$]:* At $t_1$, switch $Q_2$ is turned ON, and the proposed DCX operates in delay time mode. In this mode, because voltage $v_{\text{AB}}$ is positive, current $i_{LK1}$ increases to positive and current $i_{LK2}$ is negative, the body diode of $S_2$ and diode $D_2$ are conducted to provide current flowing paths for currents $i_{LK1}$ and $i_{LK2}$. This mode is short and ends when switch $S_2$ is turned ON at $t_2$.

*Mode 3 [$t_2$–$t_3$]:* At $t_2$, switch $S_2$ achieves ZVS turn-ON. In this mode, because the load current $i_{\text{load},n}$ is positive and the load current $i_{\text{load},p}$ is negative, the input power supply provides power for negative output through leakage inductance $L_{k2}$ and diode $D_2$.

Because the load current $i_{\text{load},p}$ is negative and capacitor $C_3$ is charged in mode 6 as shown in Fig. 14, current $i_{LK1}$ decreases from positive to negative and flows from capacitor $C_3$ to switch $S_2$ to balance the charge of capacitor $C_4$ in this mode. This mode ends when switches $Q_2$ and $S_2$ are turned OFF at $t_3$.

*Mode 4 [$t_3$–$t_4$]:* At $t_3$, switches $Q_2$ and $S_2$ are turned OFF. The proposed DCX operates in dead time mode. After switches $Q_2$ and $S_2$ are turned OFF, the output capacitor of switch $Q_2$ is charged and the output capacitor of switch $Q_1$ is discharged. Voltage across node A and node B $v_{\text{AB}}$ changes from positive to negative, thus current $i_{LK2}$ increases sharply. The body diode of $S_1$ is conducted to provide current flowing paths for currents $i_{LK1}$ and the diode $D_2$ is still conducted when current $i_{LK1}$ is negative. When the output capacitor of switch $Q_1$ is completely discharged, the body diode of switch $Q_1$ is conducted and ZVS turn-ON of switch $Q_1$ can be achieved. This mode is short and ends when switch $Q_1$ is turned ON at $t_4$.

To ensure ZVS turn-ON of switch $Q_1$, it should have

$$\frac{1}{2}\frac{L_{k1}+L_{k2}}{4n^2}[-ni_{Lk1}(t_3) + ni_{Lk2}(t_3) + i_{Lm}(t_3)]^2 + \frac{1}{2}L_m i_{Lm}(t_3)^2 > \frac{1}{2}(C_{\text{oss},Q1} + C_{\text{oss},Q2}){V_{\text{in}}}^2. \quad (18)$$

It can be observed from (18), $L_m$ is much larger than $L_{k1}$ and $L_{k2}$, and ZVS turn-ON of switch $Q_2$ can be achieved easily. If ZVS turn-ON of switch $Q_2$ can be achieved in dead time $t_{d2}, t_{d2} = t_4 - t_3$ should satisfy

$$\int_{t_3}^{t_4} [-ni_{Lk1} + ni_{Lk2} + i_{Lm}]dt > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \quad (19)$$

Because current $i_{Lm}$ can be regard as constant during $t_{d2}$, (19) can be approximated and rewritten as follows:

$$i_{Lm}(t_4)t_{d2} = \frac{V_{\text{in}}T}{4L_m}t_{d2} > (C_{\text{oss},Q1} + C_{\text{oss},Q2})V_{\text{in}}. \quad (20)$$

*Mode 5 [$t_4$–$t_5$]:* At $t_4$, switch $Q_1$ is turned ON, and the proposed DCX operates in delay time mode. Current $i_{LK1}$ is negative and current $i_{LK2}$ is positive. In this mode, the body diode of $S_1$ and diode $D_1$ are conducted to provide current flowing paths for currents $i_{LK1}$ and $i_{LK2}$. This mode is short and ends when switch $S_1$ is turned ON at $t_5$.

*Mode 6 [$t_5$–$t_6$]:* At $t_5$, switch $S_1$ achieves ZVS turn-ON. Because the load current $i_{\text{load},p}$ is negative and the load current $i_{\text{load},n}$ is positive. In this mode, the input power supply provides power for negative output through leakage inductance $L_{k1}$ and switch $S_1$.

In this mode, because the load current $i_{\text{load},p}$ is negative, voltage $v_{C3}$ increases and is higher than $v_{NS2}$. Current $i_{LK2}$ decreases from positive to zero, and diode $D_1$ achieves ZCS turn-OFF. This mode ends when diode $D_1$ is turned OFF at $t_6$.

*Mode 7 [$t_6$–$t_7$]:* At $t_6$, diode $D_1$ is turned OFF. In this mode, switches $Q_1$ and $S_1$ are conducted. Current $i_{LK1}$ still flows from capacitor $C_4$ to switch $S_1$. This mode ends when switches $Q_1$ and $S_1$ are turned OFF at $t_7$.

### C. Characteristic Analysis of the Proposed DCX

In the positive or negative half ac output current cycle of the class-D audio amplifier, dead times $t_{d1}$ and $t_{d2}$, as well as delay times $t_{d3}$ and $t_{d4}$ are very short. If $t_{d1}, t_{d2}, t_{d3}$, and $t_{d4}$ are neglected, according to volte-second balance of $L_{k1}$, it has

$$\int_0^{\frac{T}{2}} \left[\frac{nV_{\text{in}}}{2} - v_{C3}(t)\right] = \int_{\frac{T}{2}}^{T} \left[\frac{nV_{\text{in}}}{2} + v_{C4}(t)\right]. \quad (21)$$

From (21), there is

$$\int_0^{\frac{T}{2}} v_{C3}(t) = -\int_{\frac{T}{2}}^{T} v_{C4}(t). \quad (22)$$

According to (22), if voltage ripples across capacitors $C_3$ and $C_4$ are small, then the average voltage $V_{C3}$ is equal to $-V_{C4}$. Thus, output voltages of the proposed DCX is symmetric no matter what load current, which is suitable for providing bipolar supplies for the half-bridge class-D audio amplifier.

As shown in Fig. 15, the current flowing through a transformer of the *LLC* dc–dc converter and the voltage across output capacitor of the dual active bridge dc–dc converter are high-frequency pulsating. Therefore, a large capacitor is required to provide a stable output voltage in the two kinds of dc–dc converters.

In the proposed DCX, as shown in Fig. 10, if the leakage inductance of transformer, dead time and delay time as well as communication of switches are neglected, positive output voltage and negative output voltage are constant even without output capacitors because the driving signals of switches $Q1$ and $Q2$ are complementary with constant duty cycle 0.5 and the driving signals of switches $S1$ and $S2$ are complementary with constant duty cycle 0.5. The ideal equivalent circuit of the proposed DCX is shown in Fig. 16. The proposed DCX has

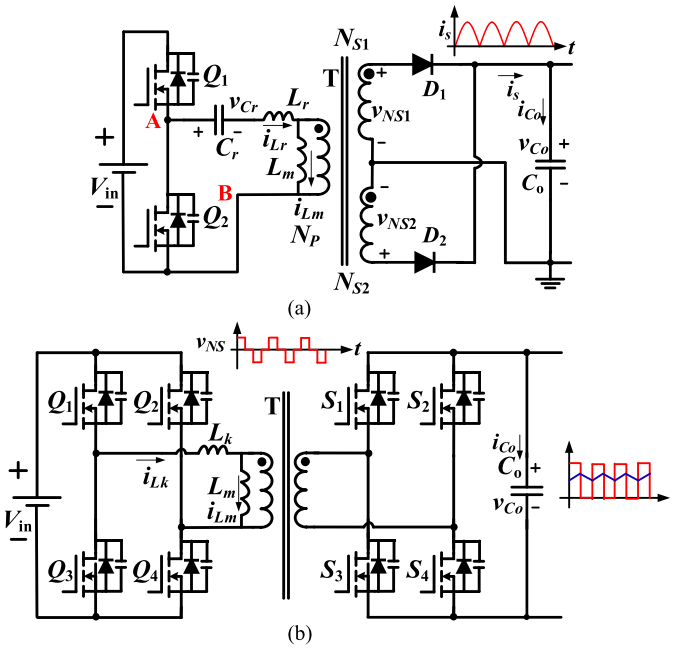


Fig. 15. Circuit diagram of the *LLC* dc–dc converter and the dual active bridge dc–dc converter. (a) *LLC* dc–dc converter in [34]. (b) Dual active bridge dc–dc converter in [21].

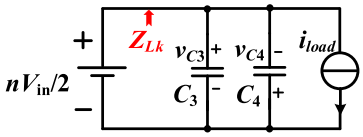

Fig. 16. Ideal equivalent circuit of the proposed DCX.

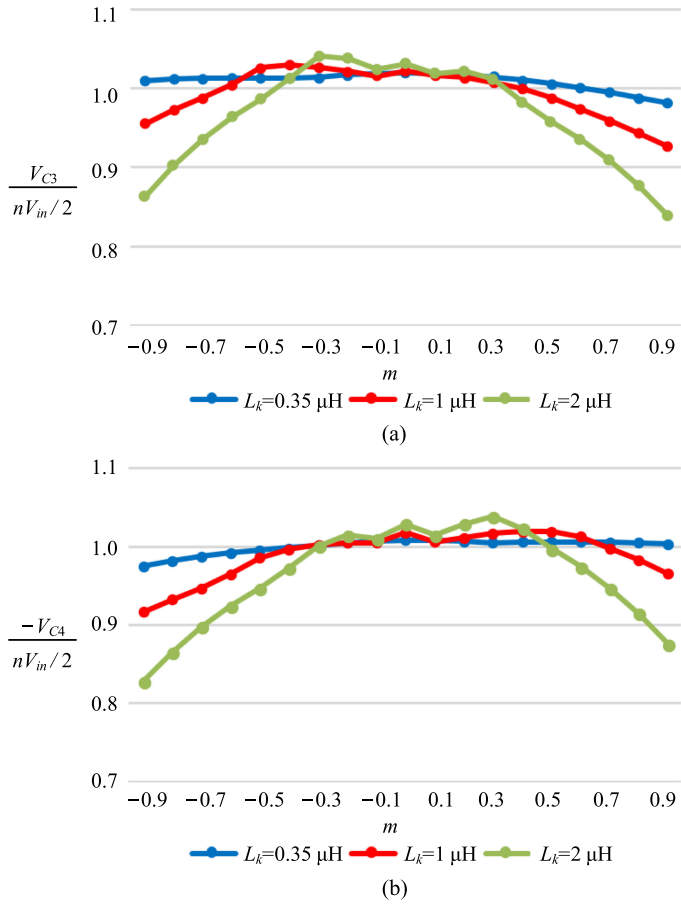


Fig. 17. Outputs voltage gains versus modulation index $m$ under different $L_{k1} = L_{k2} = L_k$. (a) $(V_{C3})/(nV_{\text{in}}/2)$.(b)$(-V_{C4})/(nV_{\text{in}}/2)$.

smooth transition between positive and negative current $i_{\text{load}}$ because input supply can be regarded as voltage source. When the switches and diodes are ideal, the leakage inductances and dead time $t_{d1}$–$t_{d2}$ as well as delay time $t_{d3}$–$t_{d4}$ are neglected, voltages $v_{C3}$ and $v_{C4}$ have no ripples. Then bipolar outputs voltage of the proposed DCX are as follows:

$$V_{C3} = -V_{C4} = \frac{nV_{\text{in}}}{2}. \tag{23}$$

In the proposed DCX, the leakage inductance $L_{k2}$ is connected with diodes $D_1$ or $D_2$, and current $i_{LK2}$ has CCM and DCM due to complex ac load current of the half-bridge class-D audio amplifier. Generally, leakage inductances are small and have limited effect on outputs voltage gains. As shown in Fig. 17, simulation positive and negative outputs voltage gains are given with different leakage inductances and load current by PSIM software. According to (8), the equivalent load current of the proposed DCX depends on modulation index $m$ when $Z_{\text{speaker}} = 4\,\Omega, \varphi = 0, \sin(\omega t) = 1$, and $V_{\text{bus}} = 54$ V. It can be seen that outputs voltage gains can be regard as constant when leakage inductances are $L_{k1} = L_{k2} = L_k = 0.35\,\mu$H.

The comparison between the proposed DCX and some other front-end dc–dc converters for the class-D audio amplifier is summarized in Table I. It can be observed from Table I, the proposed DCX has a simple controller, small output capacitors, and soft switching of all the switches with bidirectional load current.

## IV. Experimental Results

To verify the analysis results of the proposed DCX, a 200-W prototype is implemented. The circuit diagram is shown in Fig. 18. Because in the half-bridge class-D audio amplifier system, the class-D audio amplifier is close-loop and has high PSRR, the proposed DCX is open-loop and provide a probable bus voltage for the class-D audio amplifier. Thus, rectified line voltage is adopted as input power supply for the proposed audio amplifier system. In order to reduce the input voltage ripple, a smoothing capacitor $C_{\text{in}}$ is parallel with rectified line voltage.

For a 200-W class-D audio amplifier system, when modulation index $m = 1$, the minimum bus voltages of the half-bridge class-D audio amplifier should satisfy

$$\left(\frac{V_{C3,\min}}{\sqrt{2}}\right)^2 / R_{\text{speaker}} \geq P_{\text{out}}. \tag{24}$$

According to [37], the peak–peak ripple voltage across capacitor $C_{\text{in}}$ is

$$\Delta V_{\text{in,pp}} = \frac{P_{\text{out}}}{2\sqrt{2} f_{\text{in}} C_{\text{in}} V_{\text{ac}}}. \tag{25}$$

TABLE I
COMPARISON BETWEEN THE PROPOSED DCX AND SOME FRONT-END DC–DC CONVERTERS OF THE HALF-BRIDGE CLASS-D AUDIO AMPLIFIER

| References | Flyback in [8] | VDRBHB in [10] | Bidirectional DC-DC converter in [17] | Bidirectional *LLC* converter in [28] | *LLC* DCX in [32] | *LLC* DCX in [34] | Proposed DCX |
|---|---|---|---|---|---|---|---|
| Switch | 1 | 2 | 8 | 8 | 10 | 4 | 4 |
| Diode | 2 | 4 | 0 | 0 | 0 | 0 | 2 |
| Inductor | 0 | 2 | 1 | 2 | 0 | 1 | 0 |
| Transformer | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Controller | Complex | Complex | Complex | Complex | Simple | Simple | Simple |
| Output capacitor of the DC-DC converter | 1000 μF | 470 μF | - | - | - | 440 μF | 20 μF |
| Bidirectional power flowing | No | No | Yes | Yes | Yes | Yes | Yes |
| Soft switching in forward / backward mode | No / No | Yes / No | Yes / Yes | Yes / Yes | Yes / No | Yes / No | Yes / Yes |
| Input / output voltage | 110 V/48 V | 12 V/±18 V | 500 V/250 V | 75~130 V/400 V | 380 V/12 V | 400 V/12 V | 311 V/±54 V |
| Switching frequency | 25 kHz | 100 kHz | 100 kHz | 69 kHz~92 kHz | 1 MHz | 530 kHz | 200 kHz |
| Output power | 100 W | 60 W | 1 kW | 1 kW | 800 W | 300 W | 200 W |
| Efficiency | 84.04% | 88.3% | 98.2% | 97.1% | 97.6% | 97.7% | 96.3% |

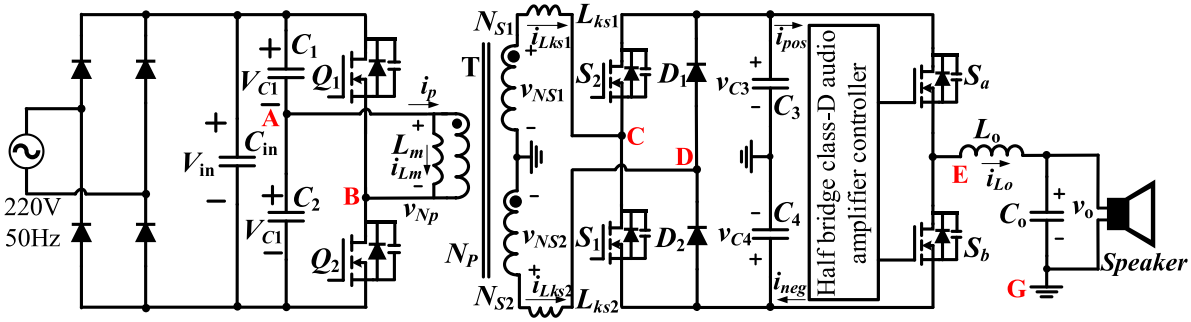


Fig. 18. Circuit diagram of the proposed half-bridge class-D audio amplifier system.

When the input voltage is minimal, (24) should be satisfied. The minimal input voltage is

$$V_{\text{in,min}} = (1 - 20\%) \cdot \sqrt{2} V_{\text{ac}} - \Delta V_{\text{in,pp}}/2. \tag{26}$$

When $V_{\text{ac}} = 220$ V, $P_{\text{out}} = 200$ W, $R_{\text{speaker}} = 4\ \Omega$, $f_{\text{in}} = 50$ Hz, from (23) and (24)–(26), it has

$$C_{\text{in}} > 198.04\ \mu\text{F}. \tag{27}$$

In this paper, $C_{\text{in}} = 220\ \mu$F is selected.

The specifications and circuit parameters are given in Table II.

Fig. 19(a) shows output voltage, positive and negative bus voltage of audio amplifier by using the converter in [10] as the front-end dc–dc converter, with $V_{\text{pos}} = -V_{\text{neg}} = 34$ V, $f_o = 20$ Hz, $R_{\text{load}} = 8\ \Omega$, $C_{\text{pos}} = C_{\text{neg}} = 50\ \mu$F and $v_o = 13.5$ V ac. It can be observed that the ripple of bus voltages is large.

Fig. 19(b) shows output voltage, positive and negative bus voltage of audio amplifier by using the proposed DCX as the front-end converter, with $V_{C3} = -V_{C4} = 54$ V, $R_{\text{load}} = 8\ \Omega$, $C_3 = C_4 = 20\ \mu$F and $v_o = 13.5$ V ac. It can be observed that the ripple of the bus voltages in the proposed DCX is much smaller than that in [10]. The results verify that the proposed DCX eliminates the power supply pumping of the half-bridge class-D audio amplifier with small DCX output capacitors.

TABLE II
SPECIFICATIONS AND CIRCUIT PARAMETERS

| | | |
|---|---|---|
| Output power, $P_o$ | | 200 W |
| Input Voltage, $V_{in}$ / Output Voltage, $V_{out}$ | | Nominal 311 V / ±54 V |
| Switching Frequency, $f_s$ | | 200 kHz |
| Capacitors $C_{in}$ | | 220 μF |
| Capacitors $C_1$-$C_2$ / $C_3$-$C_4$ | | 1 μF / 20 μF |
| Dead time $t_{d1}$=$t_{d2}$/ delay time $t_{d3}$=$t_{d4}$ | | 60 ns / 100 ns |
| Transformer | $N_p$ : $N_{S1}$: $N_{S2}$ | 20: 7: 7 |
| | Magnetizing inductance $L_m$ | 85.1 μH |
| | Leakage inductances $L_{ks1}$=$L_{ks2}$=$L_k$ (transferred to secondary side) | 0.35 μH |
| Primary side switches $Q_1$ and $Q_2$ | | FDPF20N50FT |
| Secondary side switches $S_1$ and $S_2$ | | TPH1500CNH |
| Secondary side diodes $D_1$ and $D_2$ | | ES3DB |

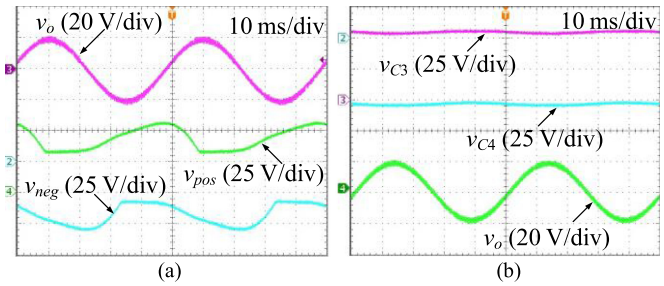


Fig. 19. Experimental waveforms of positive and negative bus voltage and audio amplifier output voltage with 8 Ω load. (a) Unidirectional converter in [10] with $V_{\text{pos}} = -V_{\text{neg}} = 34\,\text{V}$, $f_o = 20\,\text{Hz}$, $C_{\text{pos}} = C_{\text{neg}} = 500\ \mu\text{F}$ and $v_o = 13.5\,\text{V}$ ac. (b) Proposed DCX with $V_{C3} = -V_{C4} = 54\,\text{V}$, $f_o = 20\,\text{Hz}$, $C_3 = C_4 = 20\ \mu\text{F}$ and $v_o = 13.5\,\text{V}$ ac.

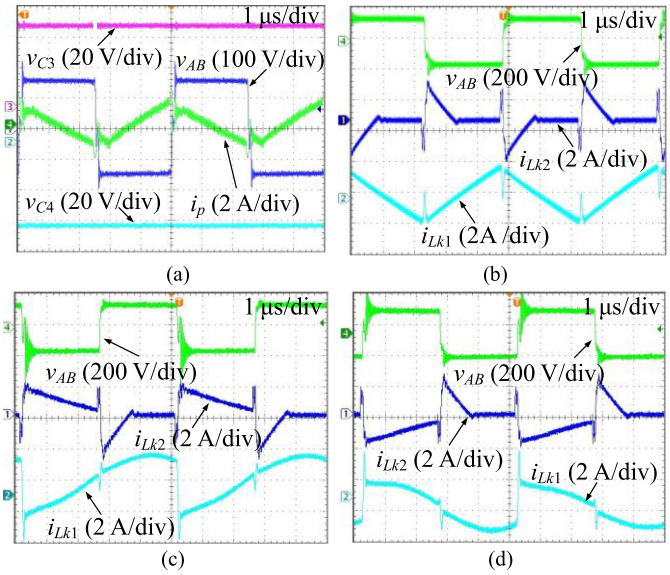


Fig. 20. Experimental waveforms of the proposed DCX connected half-bridge class-D audio amplifier. (a) Primary current $i_p$, positive and negative bus voltage $V_{C3}$ and $V_{C4}$, and the voltage across transformer primary $v_{\text{AB}}$. (b) Currents $i_{LK1}$ and $i_{LK2}$ when the half-bridge class-D audio amplifier is light load, and the voltage across transformer primary $v_{\text{AB}}$. (c) Currents $i_{LK1}$ and $i_{LK2}$ when the half-bridge class-D audio amplifier is heavy load and load current $i_{\text{load}}$ is positive, and the voltage across transformer primary $v_{\text{AB}}$. (d) Currents $i_{LK1}$ and $i_{LK2}$ when the half-bridge class-D audio amplifier is heavy load and load current $i_{\text{load}}$ is negative, and the voltage across transformer primary $v_{\text{AB}}$.

Fig. 20(a) shows primary current $i_p$, positive and negative bus voltage $V_{C3}$ and $V_{C4}$, and transformer primary voltage $v_{\text{AB}}$ of the proposed DCX connected half-bridge class-D audio amplifier. Fig. 20(b)–(d) shows transformer primary voltage $v_{\text{AB}}$ as well as currents $i_{LK1}$ and $i_{LK2}$, when the half-bridge class-D audio amplifier operates at light load, positive heavy load, and negative heavy load.

Fig. 21(a)–(l) shows drain-source voltage $V_{\text{DS}}$ and gate-source voltage $V_{\text{GS}}$ of the MOSFETs in the proposed DCX when load current is positive, zero, and negative. It can be observed that ZVS turn-ON of switches $Q_1$–$Q_2$ and $S_1$–$S_2$ are realized.

Fig. 22(a) and (b) shows the dynamic performance of the proposed audio amplifier system with a 8-Ω resistive load, under

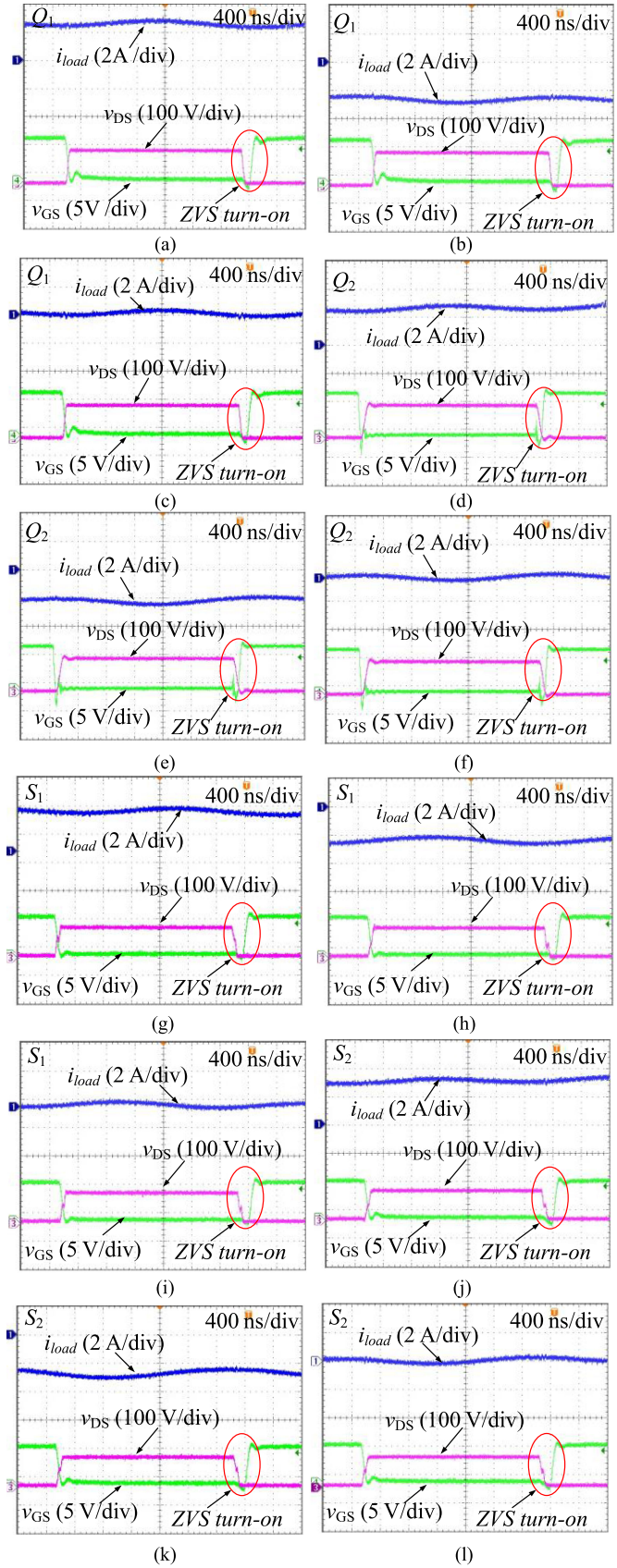


Fig. 21. Waveforms of $v_{\text{DS}}$ and $v_{\text{GS}}$ of MOSFETs in the proposed DCX.

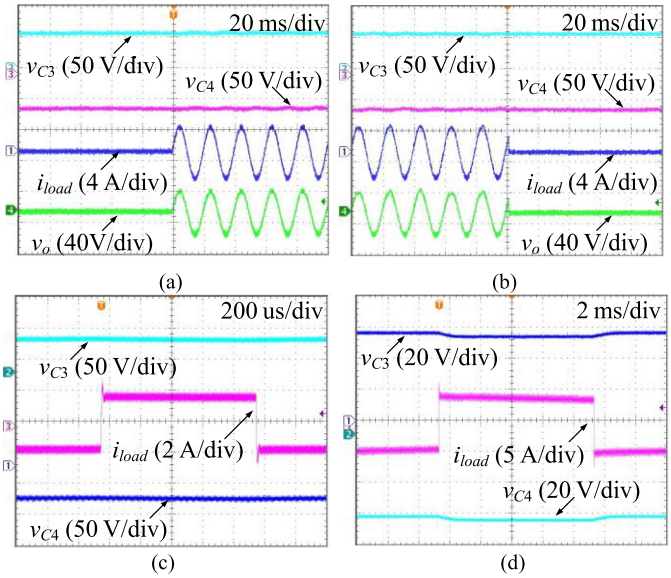


Fig. 22. Dynamic performance of the proposed DCX connected half-bridge class-D audio amplifier with resistive load. (a) Step load increase from 0 A to 2.5 A for 50 Hz sinusoidal audio amplifier output frequency. (b) Step load decrease from 2.5 A to 0 A for 50 Hz sinusoidal audio amplifier output frequency. (c) Step load between 2 A and −2 A for 500 Hz square audio amplifier output frequency. (d) Step load between 4 A and −4 A for 50 Hz square audio amplifier output frequency.

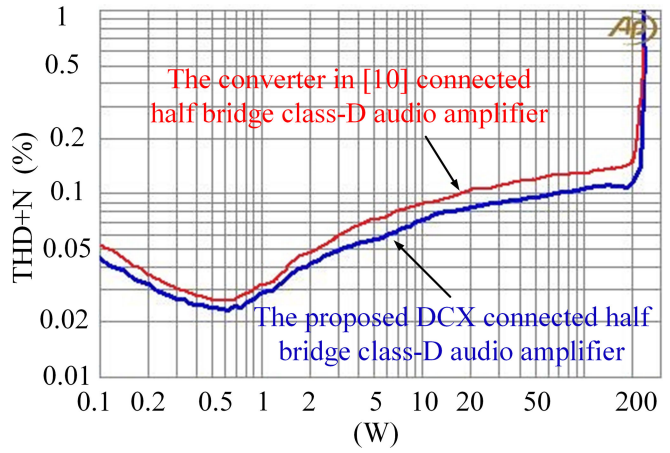


Fig. 23. Audio amplifier output voltage THD+N versus output power of the proposed DCX and the converter in [10] connected half-bridge class-D audio amplifier.

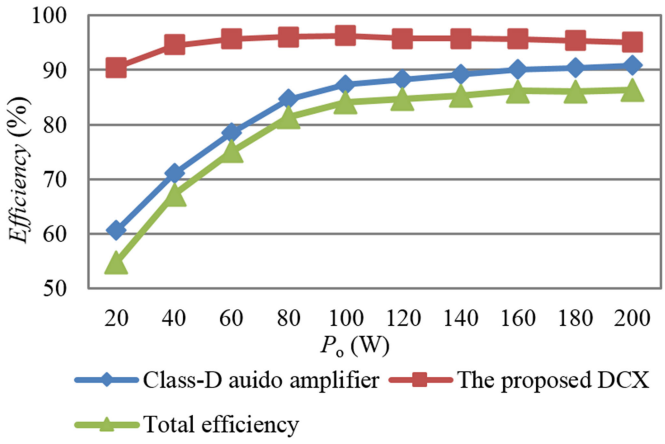


Fig. 24. Measured efficiency.

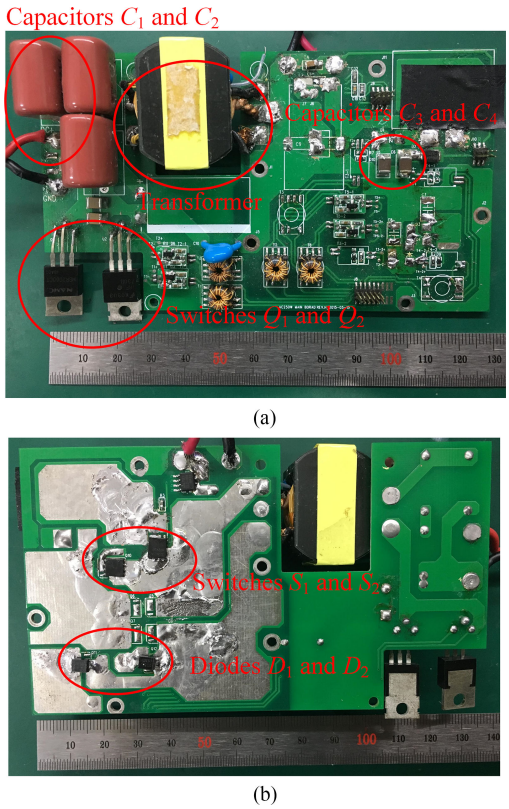


Fig. 25. Prototype of the proposed DCX. (a) Power board (Top). (b) Power board (Bottom).

step load variation from 0 A to 2.5 A, and from 2.5 A to 0 A, with the frequency of the audio amplifier output sinusoidal voltage is 50 Hz. As shown in Fig. 22(a) and (b), the output voltages of the proposed DCX are constant under step load variation of the class-D audio amplifier, which reduces power supply pumping of the half-bridge class-D audio amplifier with a small output capacitor of the DCX. Fig. 22(c) shows the dynamic performance of the proposed audio amplifier system with a 4-Ω resistive load, under step load variation from −2A to 2A, and from 2A to −2A, with the frequency of audio amplifier output square voltage is 50 Hz. Fig. 22(d) shows the dynamic performance of the proposed audio amplifier system with a 4-Ω resistive load, under step load variation from −4A to 4A, and from 4A to −4A, with the frequency of audio amplifier output square voltage is 50 Hz. As shown in Fig. 22(c) and (d), the bipolar outputs voltages of the proposed DCX are smoothing and stable relatively.

By using audio analyzer (Audio Precision 515), Fig. 23 shows the output voltage THD+N of the audio amplifier system with the proposed DCX and with the converter in [10] under different output power at 20 Hz output voltage frequency with a 4-Ω resistor load. From Fig. 23, output voltage THD+N of the half-bridge class-D audio amplifier with the proposed DCX is lower

than that with the converter in [10] because the proposed DCX eliminates the power supply pumping of the half-bridge class-D audio amplifier.

Fig. 24 shows the measured efficiency of the proposed converter. It can be observed that the highest efficiency is 96.3% at 100 W load, and the efficiency is higher than 95% over a wide load range. The proposed DCX idle loss is 2.15 W, and class-D idle loss is 4.42 W. Fig. 25 shows the prototype of the proposed DCX.

## V. Conclusion

A soft switching symmetric bipolar outputs dc-transformer (DCX) for eliminating power supply pumping of half-bridge class-D audio amplifiers is proposed. Power supply pumping of the half-bridge class-D audio amplifier is eliminated by using the proposed DCX as a front-end dc–dc converter. Compared with using a bulk electrolytic capacitor to reduce the power supply pumping and voltage stress of the half-bridge class-D audio amplifier, the proposed DCX only need small output capacitors, and thus the power density of the audio amplifier system is improved. The proposed DCX provides stable symmetric bipolar output voltages bus with small switching ripple for the half-bridge class-D audio amplifier. In addition, the proposed DCX has smoothing transition between the positive load current and negative load current with a simple open-loop controller. ZVS turn-ON of all the switches can be realized under ac load current, and thus high system efficiency is achieved in the proposed DCX.

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